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Methodically Predicting Accurate Crystal Filter Performance

When accurately modeled, crystal filter designs are predictable.

Crystal filters are predictable when accurate modeling and design techniques are used. Using an SDR-Kits network analyzer and *QucsStudio*, the measured performance of a 9 MHz 2.4 SSB band-pass crystal filter is accurately predicted. The key to successful results is appropriately modeling the crystals and accurately measuring the components.

The design uses ECS ECS-90-S-4X series crystals, which are 9 MHz series resonant crystals with a frequency tolerance of ±30 ppm. These crystals have a tighter frequency tolerance than less expensive crystals, which are usually around ±100 ppm. A ten piece lot from Digi-Key costs $0.58 each. Six crystals were randomly selected for use in the filter to demonstrate the effects of the normal crystal variation without cherry-picking the crystals based on more suitable parameters.

To use crystal filter design software, the equivalent circuit parameters of the crystal are required. An SDR-Kits vector network analyzer (VNA) was used to perform the measurements and calculate the crystal parameters.

The crystal cases may be grounded or ungrounded when constructing the filter. In this example, the crystal cases are grounded to obtain maximum isolation and prevent unwanted coupling between the crystals themselves and other circuits. Grounding the crystal case changes the transmission response of the crystal. **Figure 1** shows the parallel resonance moving higher in frequency as the crystal case is grounded as a result of the change in capacitance between the holder and the case. **Figures 2** and **3** show the details of the measurement.

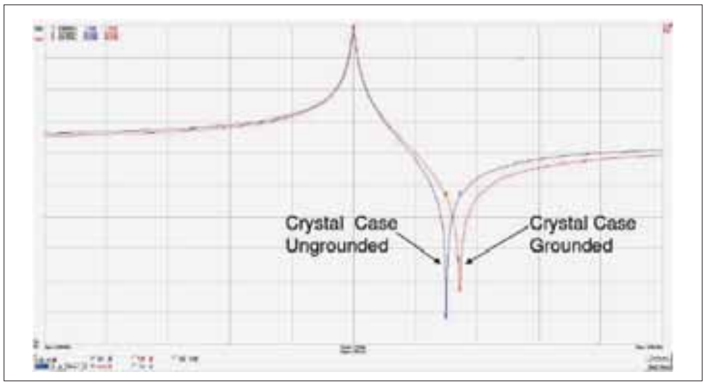


Figure 1 — Grounding the crystal case alters the parallel resonance.

Figure 4 shows the standard model for a series transmission measurement and an enhanced model, which includes the holder capacitance.

Crystal parameters can be measured using series or shunt measurement, as shown in **Figure 5**. A lot of experimentation proved that the reflection measurements yielded more accurate results than a series method. This was determined based on the agreement of simulation and measurement of constructed filters based on the crystal measurements. The reflection measurement has fewer correction terms than the through measurement on the VNA.

The VNA manual has a method of determining the holder

Figure 2 — VNA measurement setup.

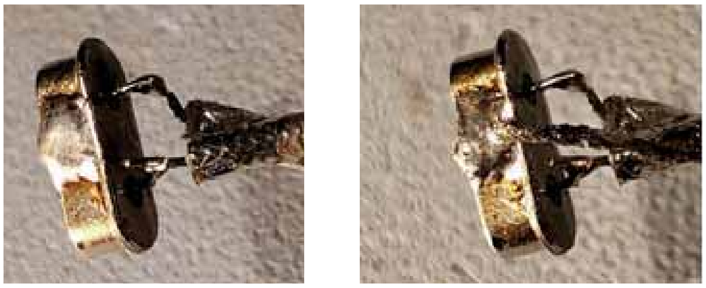


Figure 3 — Series measurement ungrounded case left, grounded case right.

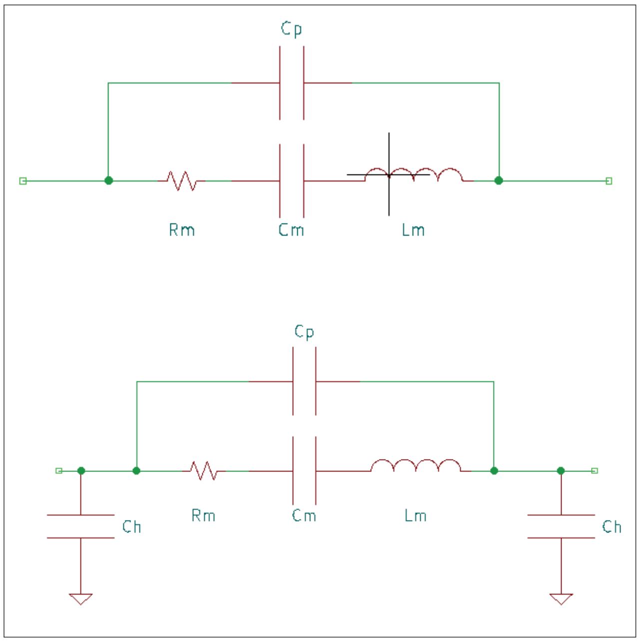


Figure 4 — Crystal models; top no holder capacitance, bottom with holder to case capacitance.

capacitance **[1]**. Instead of using the virtual ground, the crystal was measured with the case ungrounded and then grounded. **Figure 6** shows the equivalent measurement circuits.

Figure 6 also shows that the holder to pin capacitance, Ch, can then be determined as follows:

$CpGnd = Cp + Ch$

$CpUnGnd = Cp + Ch/2$

$CpGnd \times CpUnGnd = (Cp + Ch) \times (Cp + Ch/2)$

$CpGnd \times CpUnGnd = Ch/2$

$Ch = 2\ (CpGnd \times CpUnGnd).$

The actual parallel capacitance of the crystal can be determined as:

$Cp = CpGnd \times Ch.$

The crystal parameters are calculated from measurements on the SDR-Kits VNA crystal analyzer tool. Other methods could also be used as long as they provide accurate results. Great care must be taken to ensure the accuracy of the measurements, as the filter design is based on the parameters derived from the crystal measurements.

The crystals were soldered to coax pigtails because the crystal leads had been cut too short to fit into the test fixture after many experiments. The reflection calibration was then performed at the end of the pigtail. The load standard was a 0805 resistor, which was measured with an ohmmeter. Because the VNA calibration kit parameters can be entered, the load resistance does not have to be exactly 50 Ω, but the value must be accurate. A 51 Ω resistor was used for the standard. The calibration “short” was a piece of solder wick soldered across the end of the pigtail. The calibration “open” was an unterminated coax with nothing connected. Crystal cases were grounded using solder wick for these measurements. **Figure 7** shows the connection of the crystal for the series and shunt measurements. **Tables 1** and **2** show the ungrounded and grounded parameters.

The peak-to-peak frequency variation is 88 Hz for the ungrounded crystals and 90 Hz for the grounded crystals, which is 3.75% of the desired filter bandwidth. **Table 3** shows that the average calculated Ch was 0.63 pF. The actual Cp of each crystal is in place of the VNA calculated values in **Table 3**.

The 9 MHz band-pass filter described here is a 6-pole ladder filter designed for use in a receiver. The architecture is a standard ladder filter. The Steder and Hardcastle technique **[2]** and DJ6VE *Dishal* crystal filter design software are used to design the filter **[3]**.

Crystal number 2 parameters were used in the design program. That crystal was selected because the series resonant frequency was near the center, and the motional inductance was also near the average. The filter specification parameters are a 2.4 kHz bandwidth with 0.01 dB ripple. After pressing ‘calculate’, the design details are calculated and presented in **Figure 8**. The center frequency of 9001.718 kHz is based on the crystal series resonant frequency of crystal number 2. The individual crystals are tuned with series capacitors to adjust the crystal frequencies to obtain the correct filter response. The software has a tool to tune the crystals to exact frequencies for filters if desired. This is useful for loose tolerance crystals or narrow bandwidth filters. The resulting design has an input and output impedance of 711 Ω, which is determined by calculation. Input and output matching are required because the desired filter impedance is 50 Ω. The matching tool is started by selecting ‘LC-Match’ from the menu. The desired input and output impedances are preset from the filter design. Two different topologies are calculated, as shown in **Figure 9**. The Cser, Lpar design was chosen to provide a dc block to connecting circuits. **Figure 10** shows the initial design based on the *Dishal* software.

Several assumptions are made in this filter design and the presented response. The crystals are all the same frequency; all components have infinite Q; inductors and capacitors are exact values – not standard values.

Circuit analysis software was used to simulate the performance before building the

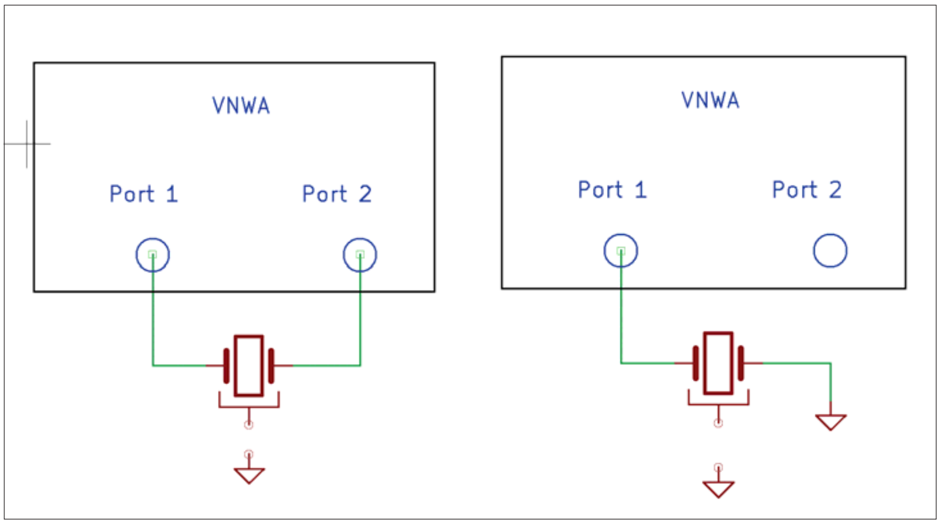


Figure 5 — Measurement methods; series measurement, left, shunt right.

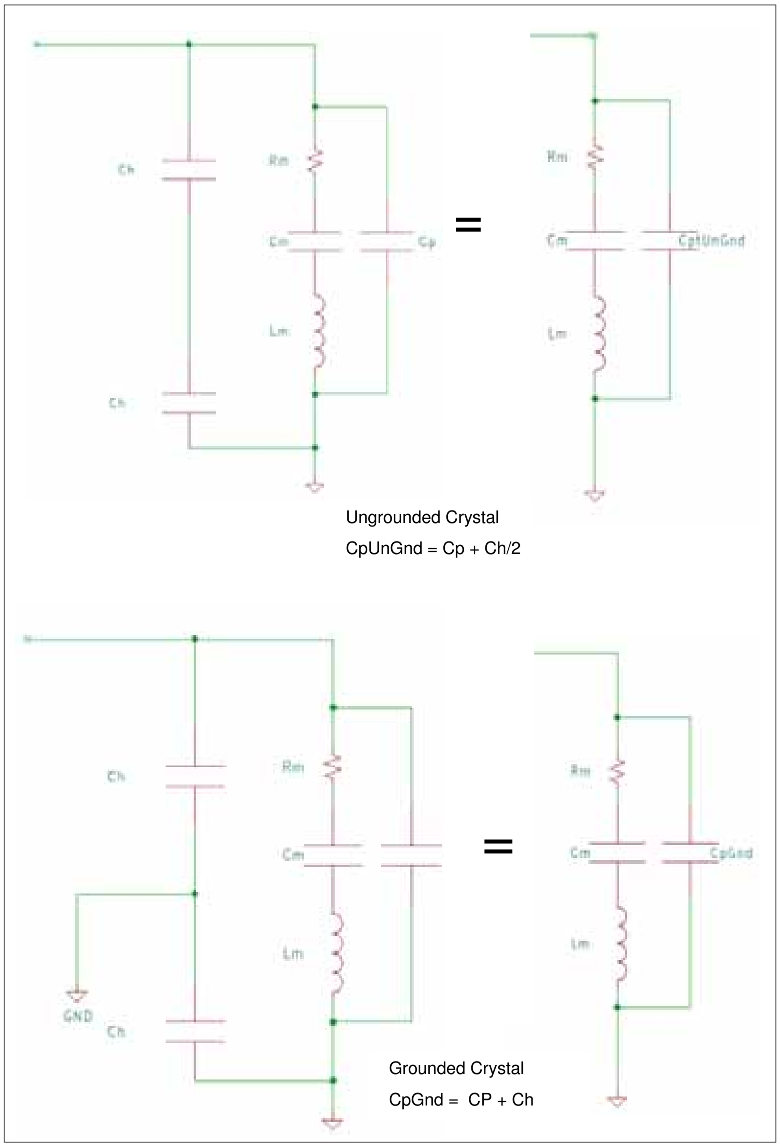


Figure 6 — Measurement models.

Figure 7 — Crystal connections; left grounded, right ungrounded.

design. This provides performance estimates based on component models, which can be adjusted to match the actual components used. The design can then be optimized by adjusting the actual real component values.

QucsStudio **[4]** is a free circuit analysis program with RF analysis capability and runs on Windows 10. There is also a predecessor *Qucs* (no *Studio*) program that is incompatible with *QucsStudio*. It does not appear to be maintained. *QucsStudio* is easy to use and has many features yet to be explored. There is a lot of documentation that can be accessed from the 'Help menu. The 'Help' documentation or a quick online search addressed any questions or issues encountered.

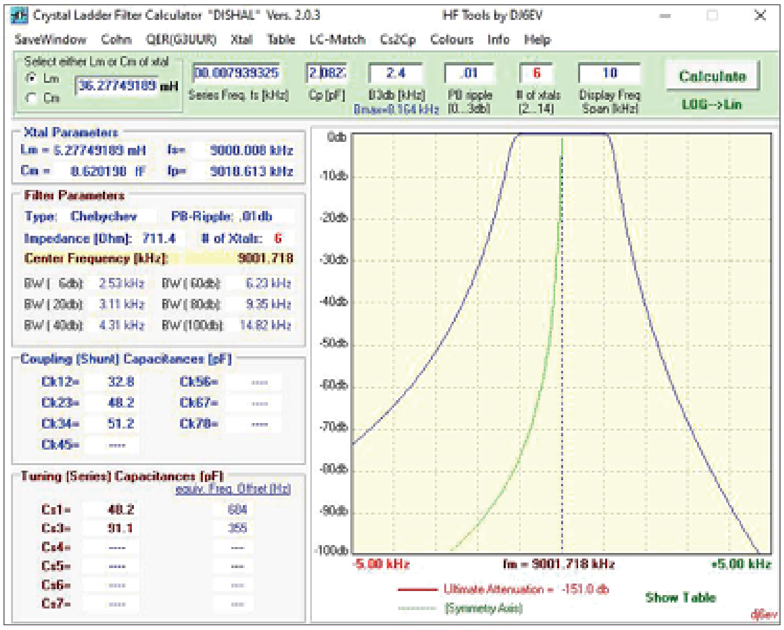
Figure 11 details the simulation for an ideal crystal filter with no Q losses (R = 0 Ω). **Figure 12** indicates that the filter has no loss, a square shape, and a 3 dB bandwidth of 2.4 kHz, as entered in the *Dishal* software what was specified to the design program. The 2 Hz simulation frequency step was achieved by setting the number of sweep points to 20001.

Next, the effect of the crystal Q is added to the simulation by setting the crystal resistance at 13.42 Ω. Insertion loss increased to approximately 1 dB, and the corners of the filter frequency response rounded and the 3 dB bandwidth is slightly narrower. Low frequency rejection did not change appreciably.

Identical crystal parameters have been used for all six crystals in the filter simulation to this point. **Figure 12** shows the response of different crystals has a slightly increased ripple. The insertion loss has increased to 1.24 dB. The bandwidth is 2.21 kHz. If a precise bandwidth of 2.4 kHz is required, a new filter with a bandwidth of

$$(2.4\ \text{kHz}/2.21\ \text{kHz}) \times 2.4\ \text{kHz} = 2.606\ \text{kHz}$$

would be specified to the filter design software and the simulation rerun with the new component values. For this



Crystal Ladder Filter Calculator "DISHAL" Vers. 2.0.3   HF Tools by DJ6EV

Select either Lm or Cm of xtal
● Lm 36.27749189 mH
○ Cm

Series Freq. fs [kHz]: 00.007939325
Cp [pF]: 2.082
B3db [kHz]: 2.4 (Bmax=0.164 kHz)
PB ripple [0...3db]: .01
\# of xtals [2...14]: 6
Display Freq Span [kHz]: 10

Xtal Parameters

Lm = 5.27749189 mH   fs= 9000.008 kHz
Cm = 0.620190 fF   fp= 9010.613 kHz

Filter Parameters

Type: Chebychev   PB-Ripple: .01db
Impedance [Ohm]: 711.4   # of Xtals: 6
Center Frequency [kHz]: 9001.718

BW [6db]:	2.53 kHz	BW [60db]:	6.23 kHz
BW [20db]:	3.11 kHz	BW [80db]:	9.35 kHz
BW [40db]:	4.31 kHz	BW [100db]:	14.82 kHz

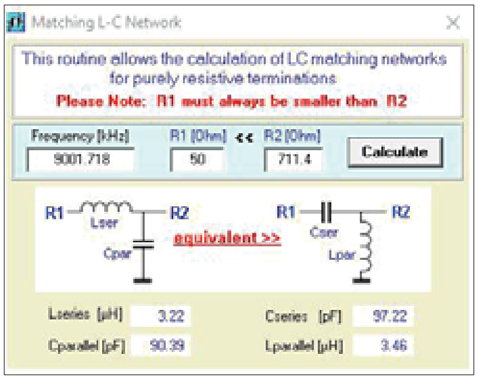
Coupling (Shunt) Capacitances [pF]

Ck12=	32.8	Ck56=	----
Ck23=	48.2	Ck67=	----
Ck34=	51.2	Ck78=	----
Ck45=	----		

Tuning (Series) Capacitances [pF]

		equiv. Freq. Offset [Hz]
Cs1=	48.2	604
Cs3=	91.1	355
Cs4=	----	---
Cs5=	----	---
Cs6=	----	---
Cs7=	----	---

Figure 8 — Filter design using *Dishal* software.



Matching L-C Network

This routine allows the calculation of LC matching networks for purely resistive terminations

Please Note: R1 must always be smaller than R2

Frequency [kHz]: 9001.718
R1 [Ohm]: 50 << R2 [Ohm]: 711.4

Lseries [µH]: 3.22
Cparallel [pF]: 90.39
Cseries [pF]: 97.22
Lparallel [µH]: 3.46

Figure 9 — Filter matching using *Dishal* software.

filter, the resulting bandwidth of 2.21 kHz is acceptable. The simulation schematic of multiple crystals is shown in **Figure 13**.

Figure 14 shows the implemented design schematic. Y3 and Y4 were swapped in position with their series capacitors in the PCB design process. The effects of circuit board trace and pad capacitance along with component measurements and estimated Qs were then simulated.

The inductor and capacitor values are adjusted to the nearest five percent standard value in order to use production tolerance components. In a few cases, a pair of capacitors was used as those values

Table 1 — Ungrounded crystal parameters.

Crystal #	F Series (kHz)	Q	Lm (mH)	Cseries (fF)	Cp (pF)	Rm (ohms)
1	9000.016994	115181	32.79398800	9.535849118	2.457333613	16.1
2	8999.994075	153651	36.28203887	8.619143909	2.426277015	13.35
3	9000.054535	130113	37.10056791	8.428871319	2.529072691	16.12
4	8999.966809	110969	35.55068393	8.796511755	2.509199437	18.12
5	9000.005303	110384	38.07669596	8.212879981	2.779623577	19.51
6	9000.015037	147213	36.06737436	8.670402631	2.547481615	13.85
Average	9000.008792	127918.5	35.97855817	8.7106097855	2.5414979913	16.175
Maximum	9000.054535	153651	38.07669596	9.535849118	2.779623577	19.51
Minimum	8999.966809	110384	32.79398800	8.212879981	2.426277015	13.35
Max – Min	0.087726	43267	5.28270796	1.322969137	0.353346562	6.16

Table 2 — Grounded crystal parameters.

Crystal #	F Series (kHz)	Q	Lm (mH)	Cseries (fF)	Cp (pF)	Rm (ohms)
1	9000.018164	113632	32.78023007	9.539848853	2.72783604	16.31
2	9000.007939	152813	36.27749189	8.620197663	2.76975980	13.42
3	9000.058117	130413	37.10510339	8.427834322	2.90848132	16.09
4	8999.967904	111733	35.43477937	8.825282352	2.77872173	17.93
5	9000.005303	110384	38.07669596	8.212879981	2.77962358	19.51
6	9000.016629	147128	36.11133077	8.659845546	2.84306427	13.88
Average	9000.012343	127684	35.96427191	.87143147862	2.8012477902	16.19
Maximum	9000.058117	152813	38.07669596	9.539848853	2.908481324	19.51
Minimum	8999.967904	110384	32.78023007	8.212879981	2.727836035	13.42
Max – Min	0.090213	42429	5.29646589	1.326968872	0.180645289	6.09

Table 3 — Holder capacitance and Cp.

Crystal #	Ungrounded Meas. Cp Series (pF)	Grounded Meas. Cp Series (pF)	Cp Series (pF) – Cp Parallel (pF)	One Lead Ch (pF)	Actual Cp (pF)
1	2.457333613	2.727836	0.27	0.54	2.186831191
2	2.426277015	2.7697598	0.34	0.69	2.082794229
3	2.529072691	2.9084813	0.38	0.76	2.149664058
4	2.509199437	2.7787217	0.27	0.54	2.239677142
5	2.779623577	2.7796236	0.33	0.66	2.120691091
6	2.547481615	2.8430643	0.30	0.59	2.251898958
Average	2.54	2.80	0.31	0.63	2.1719261115
Maximum	2.78	2.91	0.38	0.76	2.251898958

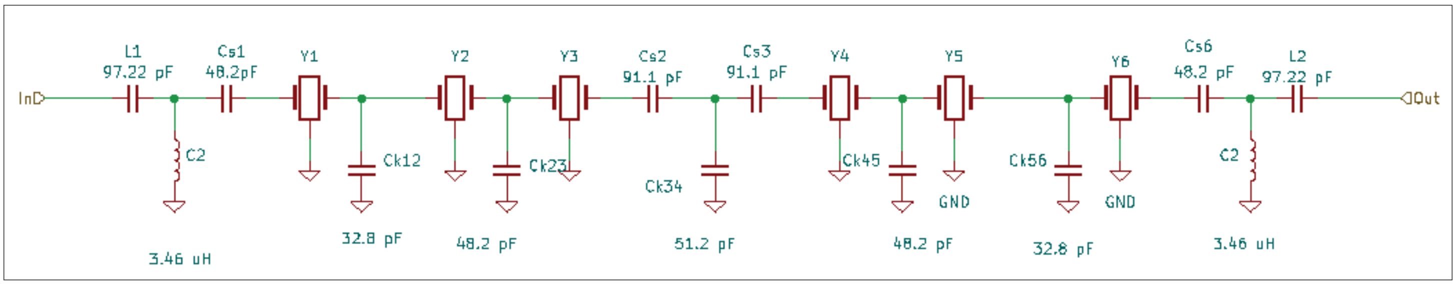


Figure 10 — Initial filter design using *Dishal* software.

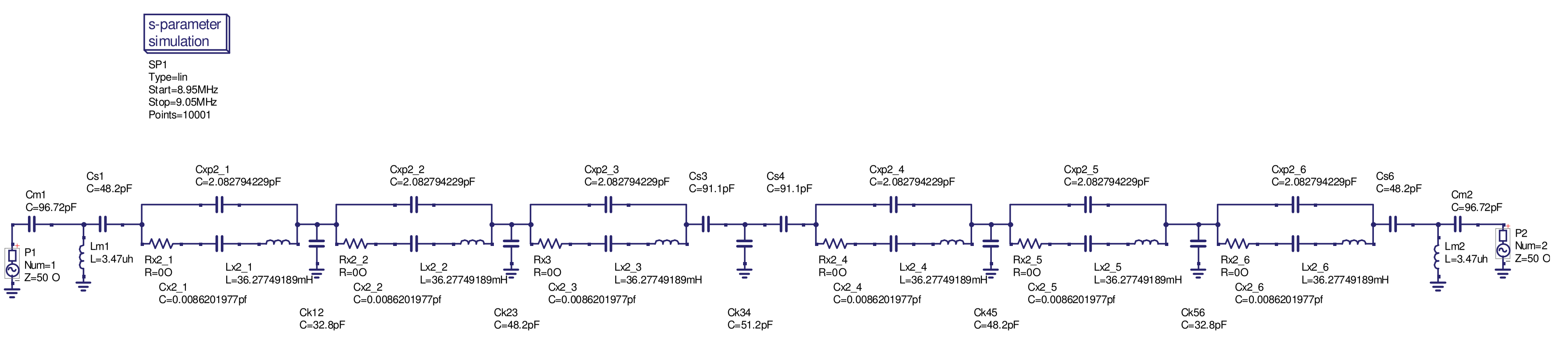


Figure 11 — Ideal Filter *QUCS Studio* simulation.

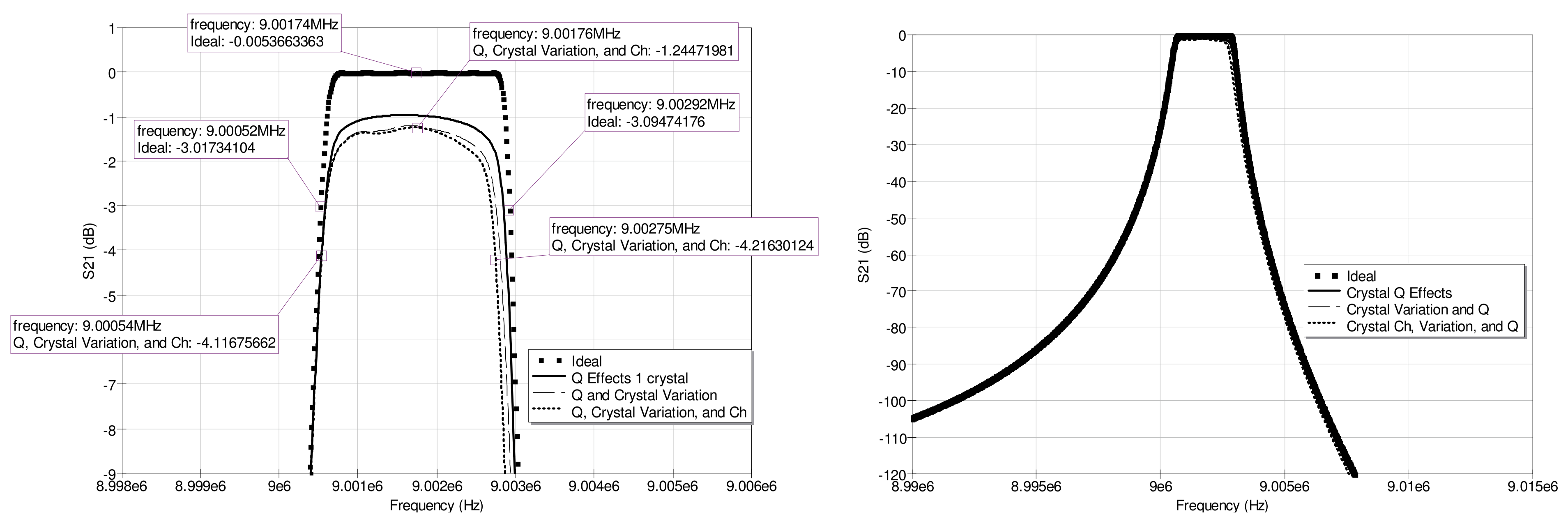


Figure 12 — Simulated crystal parameter effects bandwidth is 2.21 kHz, ideal bandwidth 2.4 kHz.

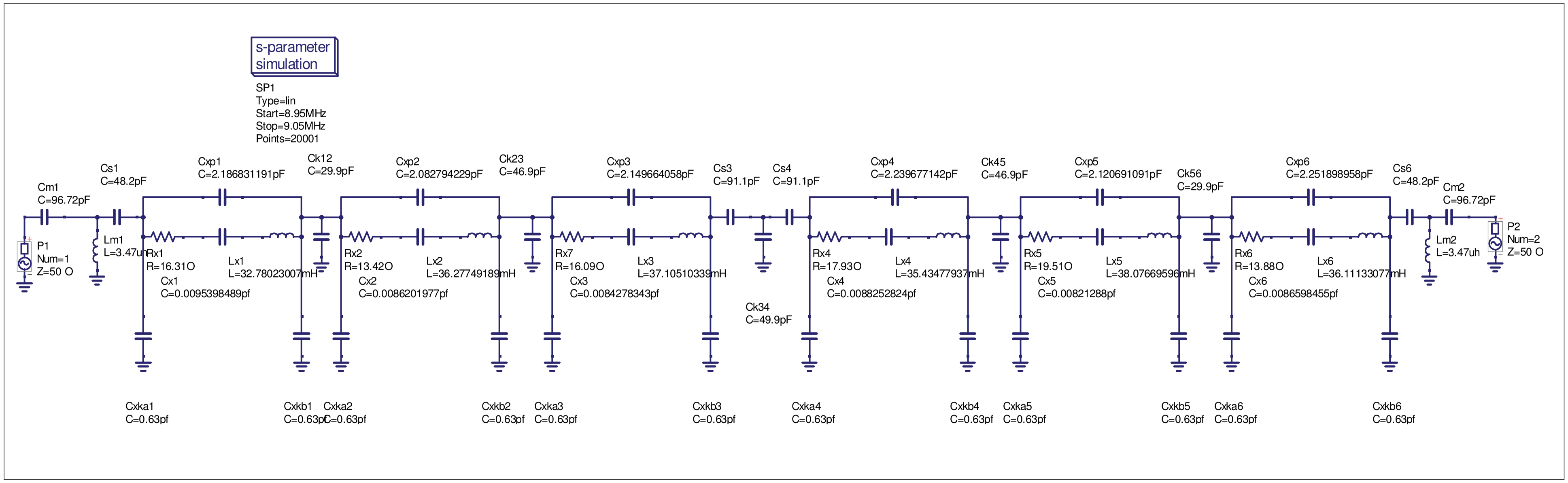


Figure 13 — Crystal holder capacitance simulation. Shunt capacitors are reduced by crystal holder capacitance.

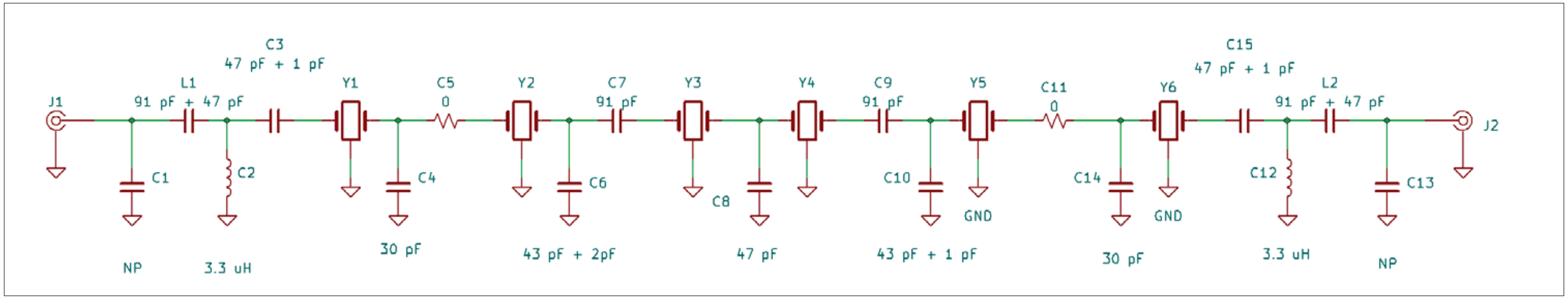


Figure 14 — Crystal holder capacitance simulation. Shunt capacitors are reduced by crystal holder capacitance.

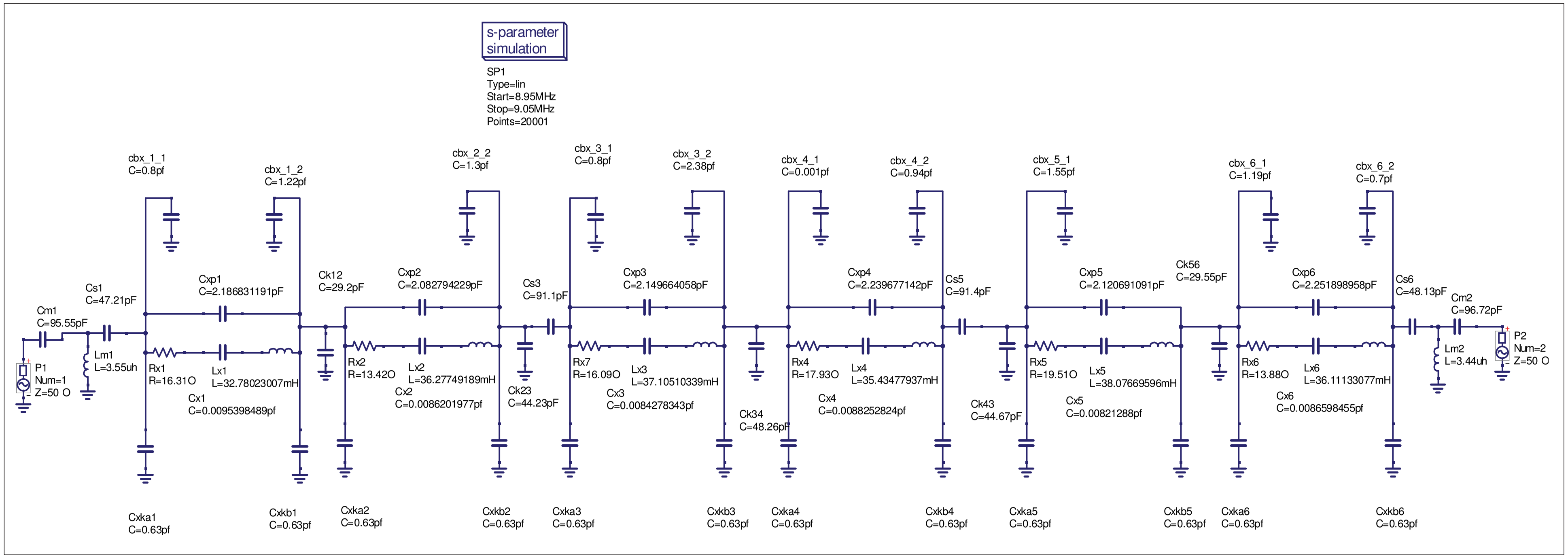


Figure 15 — Hardware implementation simulation. Includes Capacitors that are moved. PCB capacitance is included and shunt capacitors are reduced to account for PCB capacitance.

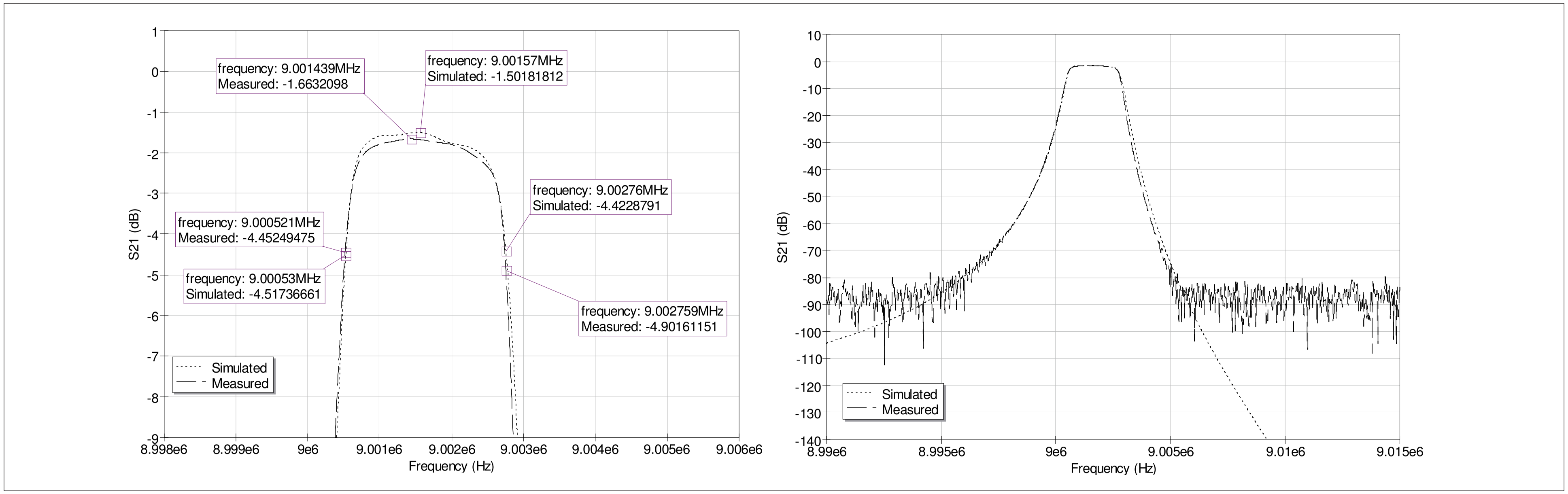


Figure 16 — PCB implementation simulated bandwidth is 2.23 kHz, measured bandwidth is 2.238 kHz.

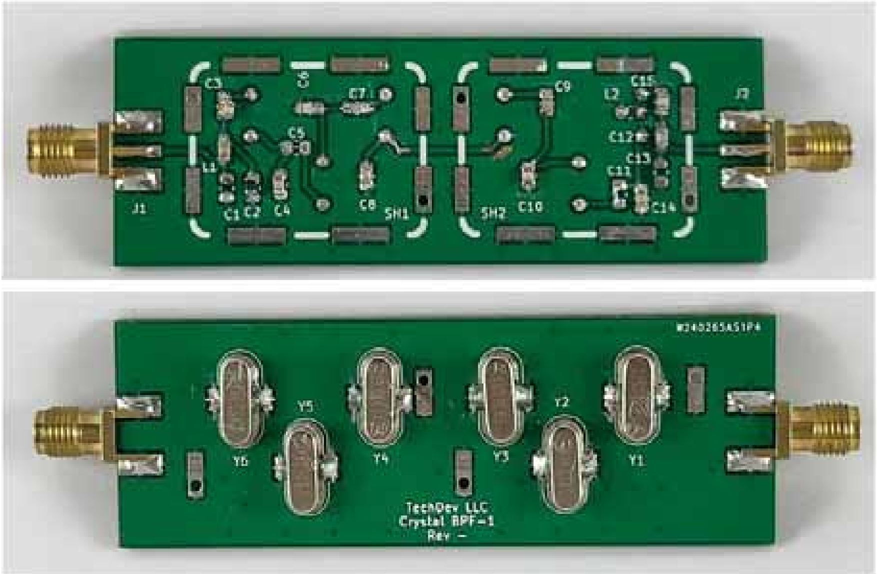


Figure 17 — Assembled crystal filter.

were on hand. This resulting upper frequency response is slightly rounded and the passband ripple increases slightly.

The filter was built on a double-sided printed circuit board, PCB. Crystals were placed on one side while the surface mount components are on the other side. Two shields were added to provide isolation between the first and second halves of the filter. A PCB provides a repeatable stray capacitance and repeatable assembly. The circuit board stray capacitance was measured at each crystal pin location and subtracted from the shunt elements in the design. The physical design including the measured values of the components, estimated component Qs and circuit board capacitance was then simulated. **Figure 14** shows physical implementation simulation schematic, including the PCB capacitance.

Real inductors and capacitors have losses, which are represented by the device Q. The 0805 inductors selected have a measured Q of 70. The *QucsStudio* inductor component has a series resistance configuration. The resistance at 9 MHz is computed as follows:

The reactance of the inductor is:

$Xl = 2\pi fL$

The Q for a series inductor is:

$Q = Xl / Rs$

Hence the series resistance can be expressed as:

$Rs = Xl / Q = 2\pi fL/Q$

Evaluating for a 3.4 μH inductor:

$L = 2\pi \times 9 \times 10^6\ \text{Hz} \times 3.4 \times 10^{-6}\ \mu\text{H} / 70 = 2.7\ \Omega.$

For a capacitor, the Q may be given in terms of the dissipation, which is 1/Q. Most of the data sheets list the dissipation as less than 0.01 or 1 percent. The capacitor Q of 300 was estimated from some inexact measurements. Better Q measurements would improve the accuracy of the simulation.

The capacitor model in *QucsStudio* uses conductance (G) instead Q so we calculate as follows:

Capacitive reactance is defined as:

$X_c = 1/(2\pi fC)$

Parallel resistance is given as:

$R_p = X_c \times Q$

Conductance is defined as:

$G = 1 / R_p$

By substitution of variables, conductance then is:

$G = 1/(X_c \times Q) = 2\pi fC / Q$

For a 39 pF capacitance, the conductance is evaluated as:

$G = 2\pi \times 9 \times 10^6\ \text{Hz} \times 39 \times 10^{-12}\ \text{pF} / 300 =$ 0.0000074 mhos.

Figures 15 and **16** depict the simulation schematic and results once the inductor and capacitor Q factors are accounted for. The predicted insertion loss is 1.90 dB while the predicted bandwidth is 2.23 kHz, which is 30 Hz wider than the simulation based without the Q factors.

Figure 17 shows the constructed filter. **Figure 16** shows the measurement of the predicted 2.23 kHz increased bandwidth. The passband traces are nearly identical, while the skirt response is a little wider on the high side. The measured insertion loss is 1.66 dB compared to 1.90 dB from the simulation. The difference is probably because of crystal measurement and Q estimation errors. The result is close enough for the intended receiver.

In conclusion, the complete implementation of a filter from initial design, simulation, construction, and performance verification has been detailed. The crystal model and filter simulation results agree with the actual crystal filter measurements.

Careful attention should be given to the following:

- Accurate measurement and modeling of the crystals. – The VNA's Shunt measurement technique was utilized.
- Accurate determination of the crystal holder capacitance from grounded and ungrounded measurements.
- Accounting for Q of the crystal as well as the tuning and matching elements.
- Accounting for the circuit board trace capacitances.
- Iteratively adjusting performance and re-simulate before construction to obtain the desired response.

Circuit boards are available on **tindie.com**, **[5]**.

Steve Geers, KA8BUW holds an Extra Class license and has been licensed since 1978. He spends his time lurking in the workshop experimenting with low cost radio projects. Steve has worked in the commercial and defense industries as an RF engineer and embedded hardware and software developer. He received a Bachelor's in Electrical Engineering from the University of Dayton and is a licensed Professional Engineer.

References

[1] **sdr-kits.net/documents/VNWA_HELP.pdf**

[2] H. Steder, DJ6EV, and J. A. Hardcastle, G3JIR, "Crystal Ladder Filters for All," *QEX* Nov./Dec. 2009, pp. 14-18.

[3] **https://www.bartelsos.de/filter/quarzfilter/quarzfilter-dj6ev**

[4] "*QucsStudio* – A Free and Powerful Circuit, Simulator," **qucs studio.de**.

[5] **https://www.tindie.com/products/techdev_steve/crystal-filter-board/**